REMARKS

Claims 1-38 are pending in the application.

Claims 1-5, 8, 9, 20-22, 24, 25, 28-31, and 38 have been rejected.

Claims 6, 7, 10-19, 23, 26, 27, and 32 have been objected to.

Claims 1-5, 10, 20, 24-25, and 28 have been amended.

Appreciation is expressed for the indicated allowability of Claims 33-37.

Objections to Claims

The Examiner has objected to Claims 6, 7, 10-19, 23, 26, 27, and 32 as being dependent upon rejected base claims. For the reasons expressed below, Applicants respectfully submit that said base claims are allowable due to argument, amendment, or both. Therefore, while Applicants appreciate the Examiner's indication that the dependent claims, in rewritten form, would be allowable, Applicants respectfully decline to amend the above dependent claims at this time, but reserve the right to do so at a later time.

Claim 2 is objected to as containing an informality related to the phrase "said switching matrix is configured to identify said switching matrix." The Office Action states that the phrase is "vague and unclear to which switching matrix it refers to." See Office Action of March 25, 2004 ("Office Action"), pp. 2-3.

In order to clarify the identity of the switching matrixes in the claims, Applicants have amended independent Claim 1 and all appropriate dependent claims, including Claim 2. Applicants have identified the switching matrix within Claim 1 as "a first switching matrix" to distinguish that switching matrix from the "plurality of switching matrixes" claimed in Claim 2 and in subsequent dependent claims. Applicants note that this amendment is made simply to improve clarity. In clarifying the claim language, these amendments are not intended to limit the scope of the claims, unless the claim language is explicitly referred to in the following arguments to distinguish over one or more of the cited references.

Rejection of Claims Under 35 U.S.C. § 112

Claims 24 and 25 are rejected under 35 U.S.C. § 112, second paragraph. Both claims have been amended to address the Examiner's concerns.

Claims 24 and 25 were rejected for insufficient antecedent basis as to the limitations of "said framing error" and "said error checker" respectively. Applicants have amended both claims to reflect dependency upon Claim 23 rather than Claim 20. Applicants note that limitations found in Claim 23 provide the antecedent basis for Claims 24 and 25.

Applicants further note that in light of the Examiner's finding that Claim 23 has been objected to but is otherwise allowable, so too should Claims 24 and 25 now be considered otherwise allowable. Applicants therefore respectfully submit that in light of the present amendment and Applicants' response to the rejection of the base independent Claim 20 below, that these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. § 102

Claims 1-5, 20-21, 28-30 and 38 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,457,556 to Shiragaki ("Shiragaki"). Applicants respectfully traverse these rejections.

Independent Claims 1, 20 and 28 all include a limitation to an error detector (or one of a plurality of error detectors) coupled to "one of said second number of outputs" (Claim 1), "one of said plurality of outputs" (Claim 20), or "one of a plurality of outputs" (Claim 28). Applicants have amended each of these claims to emphasize that the switching matrix output is selectably coupled to one of the switching matrix inputs. In addition, Claim 20 has been amended to further emphasize that the number of switching matrix outputs to which an error detector is connected is less than the total number of outputs of that switching matrix.

The Office Action suggests that the main and auxiliary fault detectors disclosed in Shiragaki anticipate the error detector of Claims 1, 20 and 28. But Shiragaki requires that the fault detector collect data "from all strategic points of the system to monitor data

streams." Shiragaki, 5:50-52. Shiragaki's fault detector "is connected to all inlet [and] outlet ports of switch 10 and to strategic points of the internal structure of the switch 10 to detect a line fault and a link failure...." Shiragaki, 5:52-55. The Shiragaki fault detector is "further connected to the outputs of all demultiplexers 12 and to the inputs of all multiplexers 14 and to strategic points of the internal structure of switch element 13 to monitor the demultiplexed data streams ...." Shiragaki, 5:58-62. Thus, Shiragaki discloses a fault detector that is connected to every switch output, along with every switch input and certain points of the internal structure of the switch, in order to be able to monitor errors within the switch.

The above amendment to the independent claims emphasizes that the error detector of the present invention is not simultaneously connected to all of the inputs and outputs of a switch matrix, but rather connected to one of the outputs and switchably connected to a selected input. By so limiting the number of inputs that can be selected by the error detector, and consequently limiting the complexity of the error detector (*see, e.g.*, Shiragaki 10:63-11:18 & Fig. 12), the present invention provides advantages to a system in which there are a plurality of such switch matrixes within a single router. By reducing circuitry and signal paths economies of cost and size are realized.

In response to Examiner's Office Action, and in the interest of economy, Applicants have amended their claims such that Claims 1, 20 and 28 are now even more clearly distinguishable over the prior art. For at least these reasons, Applicants respectfully submit that Claims 1, 20 and 28, and all claims dependent upon Claims 1, 20 and 28, are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. § 103

Claims 8 and 9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiragaki in view of U.S. Patent 6,262,820 issued to Al-Salameh ("Al-Salameh"). Claims 24-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiragaki in view of U.S. Patent 4,967,405 issued to Upp *et al.* ("Upp").

In order for a claim to be rendered invalid under 35 U.S.C. § 103, the subject matter of the claim as a whole would have to be obvious to a person of ordinary skill in

the art at the time the invention was made. *See* 35 U.S.C. § 103(a). This requires: (1) the references must teach or suggest all of the claim limitations; (2) there must be some teaching, suggestion or motivation to combine references either in the references themselves or in the knowledge of the art; and (3) there must be a reasonable expectation of success. *See* MPEP 2143; MPEP 2143.03; *In re Rouffet*, 149 F.3d 1350, 1355-56 (Fed. Cir. 1998).

For the reasons stated in the preceding section, Shiragaki does not disclose all of the claim limitations present in independent Claims 1, 20 and 28, in light of the amendments made to those claims. Nor does the Office Action suggest that either Al-Salameh or Upp provide those missing limitations. Further, Applicants are unable to find within the additional references anything related to selectably connecting an error detector from an output to an input, or a number of error detector connections less than all of the outputs of a switching matrix as required in the independent claims for the various dependent claims cited above.

Concerning the rejection of Claims 8 and 9, the Examiner admits that Shiragaki does not disclose the clock and data recovery unit of Claim 8, or specifically the phase-locked loop of Claim 9. The Office Action refers to use of a phase-locked loop to correct phase or time of a faulty signal as being known in the art, and notes that an output port to input port structure could be used in Shiragaki to this effect. *See* Office Action, p.7. The Office Action ignores that Claims 8 and 9 require only a clock and data recovery unit coupled between the output port and the error detector, and do not consider looping the signal back to the switch. Rather, the clock and data recovery unit in such an arrangement would aid in the discovery of a problem with the output signal (i.e., loss of signal or loss of frame), not correct it.

As to the rejection of Claims 22 and 31, Al-Salameh shows a system for restoring the operation of an optical switch in response to optical media failure. Al-Salameh, 9:34-10:15. Al-Salameh, however, does not provide any capacity for incrementing an error counter over an elapsed time as claimed in Claims 22 and 31. Nor does the Office Action cite to any passage in the reference for such a capacity. In light of the fact that the references, alone or in combination, do not teach all the limitations of these dependent

claims or the independent claims upon which they depend, Applicants respectfully submit that these claims are in condition for allowance.

Further, the Office Action fails to establish a motivation to combine the references. Shiragaki teaches away from a combination which would delay fault reporting to the other nodes and the fault controller. Rapid rerouting of communication paths is suggested in Shiragaki. *See* Shiragaki, 6:5-38. The delays suggested by the cited passage of Al-Salameh also call into question whether a person of ordinary skill in the art would have expected success by combining Shiragaki with the teaching of Al-Salameh.

Applicants respectfully submit that the rejections as to Claims 24 and 25 are rendered mute by the amendments to those claims, altering the dependencies of those claims from Claim 20 to Claim 23. As stated in the Office Action, and above, Claim 23 has been objected to as dependent upon a rejected base claim (Claim 20), but is otherwise allowable because the cited art does not disclose all the limitations of Claim 23. Since Claims 24 and 25 are now dependent upon Claim 23, and therefore contain the limitations of Claim 23, Applicants respectfully submit that Claims 24 and 25 are likewise allowable. Further, in light of the amendment to Claim 20, and the arguments above, Applicants also respectfully submit that these claims are in condition for allowance.

For at least the reasons stated above, Applicants respectfully submit that all of the claims currently rejected under 35 U.S.C. § 103, are now in condition for allowance and Applicants respectfully request notification thereof.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5090.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on June 23, 2004.

Attorney for Applicant(s) — Date of Signature: 6/23/2004

Respectfully submitted,

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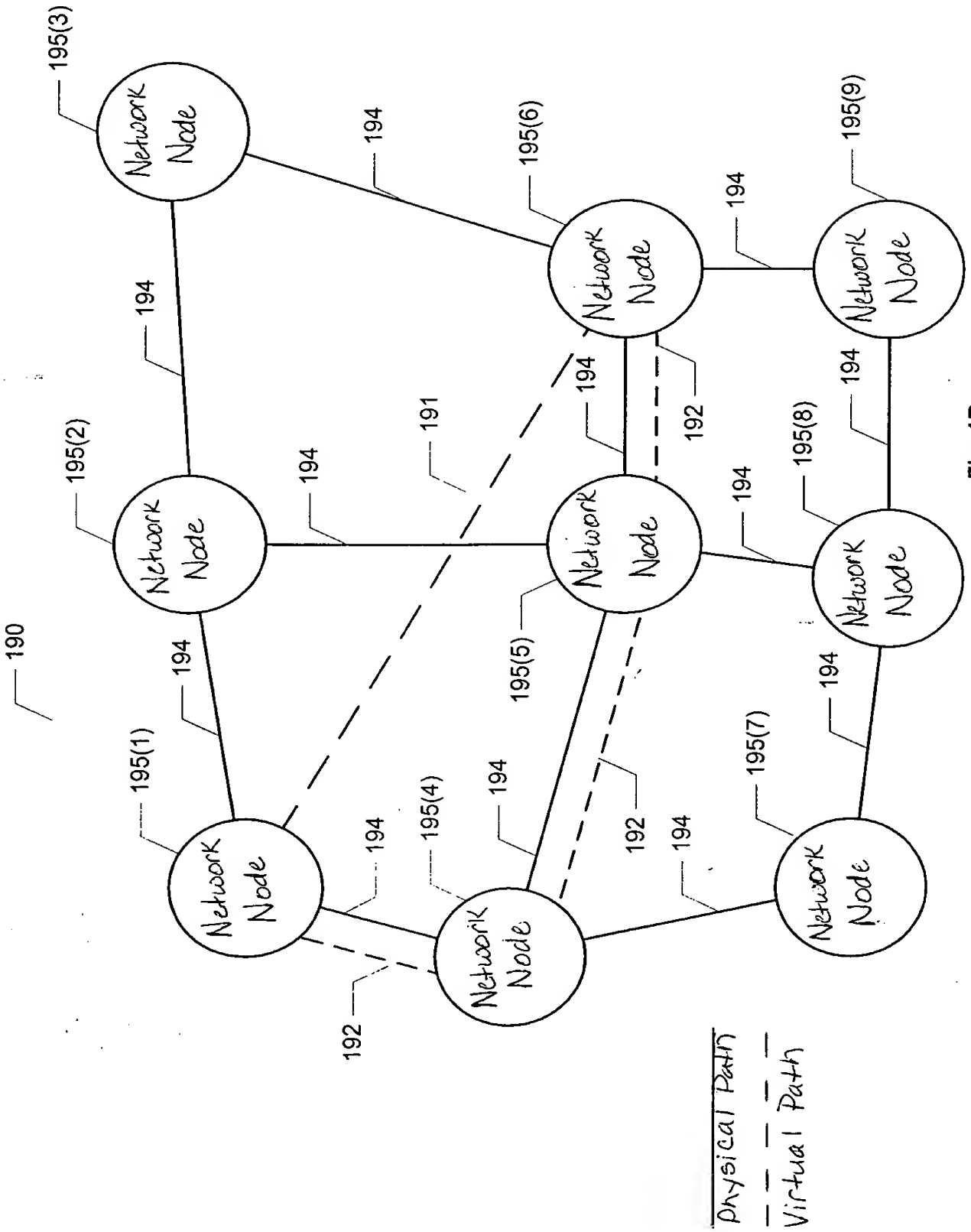

Fig. 1B